UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/827,464	04/19/2004	Simon Chu	3304.2.128	2974

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EXAMINER
KERVEROS, JAMES C

ART UNIT	PAPER NUMBER
2138	

DATE MAILED: 04/17/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/827,464	CHU, SIMON
	Examiner	Art Unit
	JAMES C. KERVEROS	2138

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 April 2004*.

2a)☐ This action is **FINAL.**   2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle,* 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-27* is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *19 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☒ All b)☐ Some * c)☐ None of:

      1.☒ Certified copies of the priority documents have been received.

      2.☐ Certified copies of the priority documents have been received in Application No. _____.

      3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *9/23/2004*.

4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

5) ☐ Notice of Informal Patent Application (PTO-152)

6) ☐ Other: _____ .

DETAILED ACTION

This is a Non-Final Action in response to the instant U.S. Application filed

4/19/2004. Claims 1-27 are pending and presently under examination.

Priority

Acknowledgment is made of applicant's claim for foreign priority under 35

U.S.C. 119(a)-(d), for TAIWAN Application N0. 092109403, filed: 04/22/2003. The

certified copy has been filed in parent Application No. 10/827,464, filed on 4/19/2004.

Specification

The abstract of the disclosure is objected to because on line 1 of the abstract, the

term "is provided" should be deleted because it is not required. Correction is required.

See MPEP § 608.01(b).

Claim Objections

Claims 1-27 are objected to because of the following informalities:

Claims 1-27 require indentation. Where a claim sets forth a plurality of elements

or steps, each element or step of the claim should be separated by a line indentation.

There may be plural indentations to further segregate subcombinations or related steps.

See 37 CFR 1.75 and MPEP § 608.01(m). Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that

form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-27 are rejected under 35 U.S.C. 102(b) as being anticipated by Lin et al. (US Patent No. 6,421,798) ISSUED: July 16, 2002.

Regarding independent Claim 1, Lin discloses a control circuit for testing memory control modules 108 seated in a respective physical memory socket 110, comprising first and second memory blocks corresponding to address space 412 and 424, Figures 3, 4 and 5, the control circuit comprising:

A processing unit (CPU 102) for executing a memory testing program specific to the first memory block 108 corresponding to the first memory socket 110, where the CPU 102 executes the memory testing program as a (test code) contained in system BIOS 104 and then transferred to the test card memory 320 on the PCI test card 114, which interfaces to an onboard test card CPU 322, and which is operable to send and receive commands and data through a PCI interface circuit 324 across the PCI bus 308 to the host CPU 102, Figures 3 and 5.

A control chip (a host bridge 304), which is part of the chipset interface 100 for interfacing to a CPU 102, physical memory modules 108 seated in a respective physical memory sockets 110, the system BIOS 104 for providing the start-up code, and the cache memory 106 interfacing directly to the CPU 102 for fast memory access, Figure 2 and 3.

Regarding independent Claim 14, Lin discloses a control circuit for testing memory control modules 108 seated in a respective physical memory socket 110,

comprising first and second memory blocks corresponding to address space 412 and 424, Figures 3, 4 and 5, the control circuit including the identical limitations as described in the independent claim 1, above.

In addition, Lin discloses host bridge 304 (comprising a memory mapping device which provides a memory mapping function), wherein the memory mapping device electrically isolates a memory bus of the one or more physical memory devices from a peripheral bus, such that removal of the one or more physical memory devices while the system is powered does not interrupt operation of the system, recited by Lin in claim 25.

Regarding independent Claim 17, Lin discloses a control method for testing a memory control module 108 seated in a respective physical memory socket 110, the memory control module 108 having an address space greater as shown in Figures 3 and 4, the control method comprising:

Dividing the memory control module 108 into a first memory block (conventional address space 412) and a second memory block (disclosed address space 424), each of the memory blocks having an address space 412 and 424 within the testing limit of the memory testing tool (test code) contained in system BIOS 104 and then transferred to the test card memory 320 on the PCI test card 114, which interfaces to an onboard test card CPU 322, and which is operable to send and receive commands and data through a PCI interface circuit 324 across the PCI bus 308 to the host CPU 102, Figures 3 and 5.

Having the first memory block (412) respond to data read/write commands asserted in response to the memory testing tool (test code) as described previously,

and having the second memory block (424) respond to the data read/write commands, as shown in a flowchart of Figure 6, including the steps of:

Loading the high-speed BIOS code is into memory locations associated with the run-time BIOS address space 434 of PCI address space 428, (block 602).

Reading the BIOS code is from the memory locations associated with the PCI address space 428 into the cache memory 106, (block 606).

Running the high-speed code from the cache memory 106 to execute test patterns on the physical memory 108 under test, (block 608).

Regarding Claims 18, 19, the first and second memory blocks corresponding to address space 412 and 424 are identical, wherein the memory testing tool (test code) is specific for testing the first memory block, as shown by the flowchart of Figure 6.

Regarding Claims 2, 5, 6, 16, 25-27, Lin discloses control chip (host bridge 304) accessing the first memory block 108 corresponding to the first memory socket 110 in response to the data read/write commands from the (CPU 102). The system includes a chipset interface 100 for interfacing to a CPU 102, physical memory modules 108 seated in a respective physical memory sockets 110, the system BIOS 104 for providing the start-up code, and the cache memory 106 interfacing directly to the CPU 102 for fast memory access. The bus interfaces 112 have data, address, and control lines for carrying such signals to the respective devices.

Regarding Claim 3, 20, Lin discloses host bridge 304 (comprising a memory mapping device which provides a memory mapping function), wherein the memory mapping device electrically isolates a memory bus of the one or more physical memory

devices from a peripheral bus, such that removal of the one or more physical memory

devices while the system is powered does not interrupt operation of the system, recited

by Lin in claim 25.

Regarding Claim 4, 15, Lin discloses processing unit (CPU 102) and the control

chip (host bridge 304) are a central processing unit and a north bridge chip of a

computer system, the mapping circuit is part of (host bridge 304), as shown in Figure 3.

Regarding Claims 7-11, 21-23, Lin discloses a block diagram of system address

space as implemented by conventional systems and a disclosed embodiment, as

shown in Figure 4. The conventional boot-up process runs code directly from the BIOS

flash ROM 104. In this particular embodiment, a chipset 100 is provided which can

map an address from an address space 400 of a CPU to memory space having four-

gigabytes of potential memory locations, this typically referred to as physical memory

space.

Regarding Claims 12, 13, 24, Lin discloses a system BIOS 104 responsible for

booting the computer by providing a basic set of instructions. The BIOS code has been

modified such that after start-up, the PCI card 114 enables the memory power switch

116 to drop power only to the physical memory 108 such that it may be pulled from its

memory slot 10 and replaced while the computer system is running, precluding the

need to power down the system to replace the memory for testing. This is

accomplished by not running the system BIOS code from the physical memory 108, but

from PCI memory space using a coordinated effort of the system BIOS 104, cache

memory 106, and the PCI card 114.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JAMES C. KERVEROS whose telephone number is (571) 272-3824. The examiner can normally be reached on 9:00 AM TO 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.
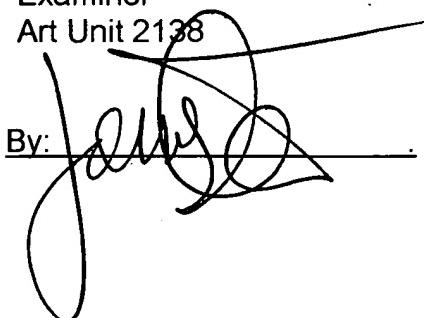
Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JAMES C KERVEROS
Examiner
Art Unit 2138

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